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JC598 U.S. PTO 01/13/99

January 13, 1999

Assistant Commissioner for Patents
Washington, D.C. 20231

Attorney Docket No. OKI 4646.01

ATTENTION: Box PATENT APPLICATION

Re: New Patent Application
Inventor(s): Yasutaka SAKAINO, Jouji KATO and
Yoshiaki UMEZAWA

Sir:

Please find attached hereto an application for patent which includes:

Specification, Claims, Abstract of the Disclosure, Declaration, Power of Attorney and Information Disclosure Statement with Form PTO-1449.

Priority Documents, the rights of priority of which are claimed herewith under 35 U.S.C. 119:

Japanese Appln. No. 021021/98 filed January 23, 1998.

Drawings: 6 Sheets Formal Drawings (Figs. 1 - 6)

Fee (see formula below) - Check Enclosed:

Basic Fee $760.....	$760.00
Additional Fees:	
Total number of claims in excess of 20 0 times $22	$ -0-
Number of independent claims 4 (1, 3, 6 and 14) in excess of 3: 1 times $78.....	$ 78.00
Multiple Dependent Claim $135/270.....	$ -0-
An assignment and cover sheet is likewise enclosed; Recording Fee.....	$ 40.00
TOTAL FEES FOR THE ABOVE APPLICATION...	$878.00

In the event there is attached hereto no check, or a check for an insufficient amount, please charge the fee to our Account No. 19-3700 and notify us accordingly.

Respectfully submitted,

Robert J. Frank
(Registration No. 19,112)

RJF:jh

Semiconductor Integrated Circuit

BACKGROUND OF THE INVENTION

Technical Field

The present invention relates to a semiconductor integrated circuit, and particularly to a layout pattern for a semiconductor integrated circuit.

Related Art

Conventionally, transistors utilizing high resistance polysilicon wiring have been used in MOS transistors that have to be protected against static electricity surges in the vicinity of pads of input protection circuits and output circuits, and surge voltage is relieved by utilizing resistive components of the polysilicon wiring.

Fig. 3 is a circuit diagram of an output circuit. Fig. 4-B is a layout pattern drawing of an NMOS transistor having conventional circuitry, and Fig. 4-A schematically shows a cross section of Fig. 4-B. The output circuit and the layout will now be described below using the drawings.

In the output circuit, the NMOS transistor 301 has a gate connected to an output terminal 302 from an internal circuit, a drain connected to an output terminal 303 and a source connected to GND 304. This NMOS transistor 301 is in a conducting state when a signal supplied to the gate is at an H level. At this time, an L level signal is output from the output terminal 303. When the signal supplied to the gate is an L level, the NMOS transistor 301 is in a non-conducting state, and at this time an H level signal is output from the output terminal 303.

The conventional pattern layout of an NMOS transistor used in this type of circuit will be described in more detail.

As shown in Fig. 4-A, the NMOS transistor has part of a source 405 connected to a polysilicon wiring layer 402 arranged on a source region, via a first contact 401.

The polysilicon wiring layer 402 is connected to a first metal layer 403 arranged on the same source 405 region, via a second contact 404. The first

metal layer 403 is connected to GND.

Part of the drain 406, similarly to part of the source 405, is connected to the polysilicon wiring layer 402 arranged on a drain region, via the first contact 401. The polysilicon wiring layer 402 is connected to a first metal layer 403 arranged on the drain 406 region, via a second contact 404. The first metal layer 403 is connected to an output terminal.

Here, the contact 401 and the contact 404 are arranged so as to alternate, as shown in Fig. 4-B.

In the above described conventional circuit, the first contact 401 and the second contact 404 are alternately arranged without considering the difference between the resistance value of the first contact 401 and the resistance value of the second contact 404. Accordingly, the total resistance value of all the contacts will become large. There is thus a problem that the I-V characteristic of the MOS transistor will be degraded by this increase in the resistance value of the contact portions.

SUMMARY OF THE INVENTION

An object of the present invention is to lower the overall resistance value. According to an example of the present invention, there is provided a semiconductor integrated circuit device, comprising, impurity diffusion regions formed as source and drain on a semiconductor substrate; a first conduction layer having a first resistivity formed on the impurity diffusion regions; a first contact hole group connecting the first conduction layer and the impurity diffusion region; a second conduction layer having a second resistivity formed on the first conduction layer; and a second contact hole group connecting the first conduction layer and the second conduction layer at an upper part of the impurity diffusion region, and wherein the total number of contact holes is respectively different between the first contact hole group and the second contact hole group.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a layout drawing showing a pattern layout of a first embodiment of the present invention.

Fig. 2 is an I-V characteristic drawing showing improved characteristics brought about by the present invention.

Fig. 3 is a circuit diagram of an output circuit.

Fig. 4 is a layout drawing showing a pattern layout of the related art.

Fig. 5 is a circuit diagram of an input circuit.

Fig. 6 is a layout drawing showing a pattern layout of a second embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

(First Embodiment)

A circuit diagram showing an output circuit of a first embodiment of the present invention is the same as Fig. 3. As shown in Fig. 3, the NMOS transistor 301 of the output circuit has a gate connected to an output terminal 302 from an internal circuit, a drain connected to an output terminal 303 and a source connected to GND 304. This NMOS transistor 301 is in a conducting state when a signal supplied to the gate is at an H level. At this time, an L level signal is output from the output terminal 303. When the signal supplied to the gate is an L level, the NMOS transistor 301 is in a non-conducting state, and at this time an H level signal is output from the output terminal 303.

Fig. 1 is a drawing showing a pattern layout used in the case of the present invention. The layout structure of an NMOS transistor of the present invention will now be described below using Fig. 1.

A polysilicon layer 102, constituting a first high resistance wiring layer, and a first metal layer 103, constituting a second low resistance wiring layer, are formed on respective regions of a source 105 and a drain 106.

Parts of the source 105 and drain 106 of the NMOS transistor are connected to the first wiring layer, being the polysilicon later 102, via a plurality of first contacts 101. The first contacts are each formed having a size of 0.6 μm by 0.7 μm. A contact resistance between the source or drain and the first wiring layer is 170 Ω/unit in terms of a sheet resistance.

The first wiring layer, being the polysilicon layer 102, and the second wiring layer, being a first metal layer 103, are connected via a plurality of second contacts 104. The first contacts are each formed having a size of 0.7 μm by 0.7 μm. A contact resistance between the first wiring layer 102 and the second wiring layer 103 is 9.5 Ω/unit in terms of a sheet resistance.

Here, the contact resistance of portions of the source region 105 and the drain region 106 where the first contacts 101 are formed is larger than the contact resistance of portions where the second contacts 104 are formed.

As shown in Fig. 1, with respect to the pattern layout of the present invention, in order to lower the overall resistance, a plurality of first contacts 101 are arranged inside the area between the second contacts 104. In this embodiment, five first contacts 101 are arranged between two second contacts 104. An interval L1 between each first contact 101 is set to a fixed value of 1 μm.

The distance L2 when a first contact 101 is adjacent to a second contact 104 is also a fixed value, and in Fig. 1 it is 1 μm.

A distance L3 is a distance from the edge of the source 105 or drain 106 to a first contact hole 101, and distance L4 is a distance from a gate electrode to a first contact hole 101, and the first contact holes are arranged so that $L3 \geq L4$. In this embodiment, $L3 = L4 = 5.25$ μm.

The first metal layer 103 on the source region 105 is connected to GND, while the first metal layer 103 on the drain region 106 is connected to an output terminal.

The operation of the first embodiment of the present invention will be described below. The characteristic of drain current against drain voltage for the NMOS transistor (I-V characteristic) is shown in Fig. 2. The characteristic shown in Fig. 2 is a characteristic for the case where the ON resistance of the NMOS transistor 301 of Fig. 3 is 30.

If a layout pattern such as that in Fig. 1 is used, the resistance of the first contacts is 34 Ω (170/5) and the resistance of the second contacts is 4.8 Ω (9.5/2). Accordingly, the ON resistance of the NMOS transistor becomes 30 + 34 + 4.8 = 68.8 Ω. The drain voltage at which the NMOS transistor actually operates is approximately 1.6V. With the drain voltage at 1.6V in this case, a

current of 23.3 mA flows.

On the contrary, if the I-V characteristic is measured using the conventional pattern layout shown in Fig. 4-B, the resistance of the first contacts is 56Ω (170/3 and the resistance of the second contacts is 2.4 Ω (9.5/4).

The overall ON resistance becomes 30 + 56 + 2.4 = 88.4 Ω. In other words, with the drain voltage at 1.6V, a current of only 19 mA will flow.

With an I-V characteristic in a hypothetical ideal state where there is absolutely no contact resistance, a current of 52.8 mA will flow with a voltage of 1.6V. With the NMOS transistor using the pattern layout of the present invention, a current reduced to 44% compared to that of this ideal state will flow. Compared to this, a current flow in an NMOS transistor using the conventional pattern layout is reduced by more than 64%.

By using the present invention, an improvement of 20% can be expected. In order to thus reduce the overall contact resistance, a plurality of first contacts 101 are arranged inside the area between the second contacts 104. As a result, compared to the related art, The overall contact resistance of the NMOS transistor is reduced, and the current driving capability is improved.

Since a plurality of first contacts 101 are arranged between the second contacts 104, overall, current will flow in either of the first wiring layer of the second wiring layer in a well balanced manner.

By setting the interval between the multiply arranged first contact 101 to a predetermined fixed interval, the length of polysilicon wiring layer 101 between each contact 101 is equal. That is, the individual resistance of the polysilicon layer between the contacts 101 is equal. As a result, a surge voltage is uniformly distributed and overall protection against surge voltages is stable, even if a surge such as static is temporarily input to the output terminals.

The first contact holes are arranged so that a distance L3 from the edge of a source 105 or drain 106 to a first contact hole 101, and distance L4 from a gate electrode to a first contact hole 101 satisfy $L3 \geq L4$. When surges such as static are input, the surge voltage will be converged on a portion located between an edge of the diffusion region and a first contact 101 extremely close to the edge, and there is no fear of damage to the diffusion region .

(Second Embodiment)

Fig. 5 is a circuit diagram showing an input/output circuit of the second embodiment of the present invention. As shown in Fig. 5, an NMOS transistor 510 in the output circuit has a gate connected to an output terminal 503 from internal circuitry 503, a drain connected to an input output terminal 501, and a source connected to GND 504. The NMOS transistor 510 is in a conducting state when an H level signal is supplied to the gate. At that time, an L level signal is output from the input/output terminal 501. When an L level signal is supplied to the gate, the NMOS transistor 510 is in a non-conducting state, and an H level signal is output to the input/output terminal 501.

The NMOS transistor 520 in the input circuit has a drain connected to the input/output terminal 501, and the source and gate are connected to GND 504. This NMOS transistor 520 functions as a protection element to shunt static surges etc., to the NMOS transistor 510 in the output circuit, and to the input/output terminal 501, to GND 504.

Fig. 6-A and Fig. 6-B respectively show pattern layouts for the NMOS transistor 510 and the NMOS transistor 520 in Fig. 5. The transistor layout structure of the present invention will be described below using Fig. 5 and Fig. 6.

As shown in Fig. 6, in the NMOS transistor 510 of the output circuit side in Fig. 5, a gate electrode 619 having a gate length LG of 0.9 μm is formed on an active region of the NMOS transistor 510. A polysilicon layer 612 constituting a first high resistance wiring layer, and a first metal layer 613 constituting a second wiring layer are formed on the active region of the source 615 and the drain 616.

The source 615 and drain 616 of the NMOS transistor are respectively connected to the polysilicon layer 612, being the first wiring layer, through a plurality of first contacts 611. The first contacts are formed having a size of 0.6 μm by 0.7 μm.

The polysilicon layer 612, being the first wiring layer, is connected to the first metal layer, being the second wiring layer, through a plurality of second contacts 614. The second contacts 614 are formed having a size of 0.6 μm by

0.7 μm.

Here, the contact resistance of the source region 615, drain region 616 and the part where the first contacts 611 are formed, is larger than the contact resistance of the portion where the second contacts 614 are formed.

As shown in Fig. 6, with the pattern layout of the present invention, the first contacts 611 are multiply arranged at fixed intervals between the second contacts 614, so as to reduce the overall contact resistance. In this embodiment, the second contacts 614 are arranged at three places, and four first contacts are respectively arranged in portions positioned between neighboring contacts 614. An interval L1 between adjacent first contacts has a fixed value of 1 μm.

The contacts are arranged so that a distance L2 between an adjacent first contacts and second contact is always equal, and in this embodiment it is 1 μm. A distance from the edge of the source region 615 or drain region 616 to a first contact 611 is termed L3, while a distance from a gate electrode to a contact is termed L4, and the contacts are arranged to satisfy the relationship $L3 \geq L4$. In this embodiment $L3 = L4 = 5.25$ μm.

In the input circuit side NMOS transistor 520 of Fig. 5, as shown in Fig. 6-B, a gate electrode 629 having a gate length LG of 0.9 μm is formed on an active region 620 of the NMOS transistor 520. A polysilicon layer 622 constituting a first high resistance wiring layer, and a first metal layer 623 constituting a second wiring layer are formed on the active region of the source 625 and the drain 626.

The relationship between the first and second contacts and the respective wiring layers is the same as the relationship in the output circuit. The input circuit side differs from the output side only in that because the width of the active region is wider than the output circuit part, the number of second contacts is different from that on the output side, and second contacts are arranged at four places.

Specifically, an interval L1 between adjacent first contacts is the same as an interval set in the transistor formed in the output circuit, and in this embodiment it is fixed at 1 μm. An interval between first contacts and second contacts is also exactly the same as the interval set for the transistor formed in the output circuit, and that is also 1 μm in this embodiment.

A detailed description will be given below of the operation when a static surge, as previously described, is applied to the input/output terminal 501 of Fig. 5.

When a negative voltage of -1000V, caused by static electricity etc., is applied to the input output terminal 501 in Fig. 5, the NMOS transistors 510 and 520 are both in an ON state. The applied static electricity is shunted by the flow of current from GND to the input/output terminal 501.

When there is disparity between the input circuit side NMOS transistor 520 and the output circuit side NMOS transistor 510, the current for diverting the applied voltage will flow more in one transistor that the other. If more current flows in one transistor than the other, the load will be concentrated in the side having the increased current flow. Accordingly, protection of the overall circuit against static electricity etc. is lowered.

In the second embodiment, as has been described above,the gate lengths have been made equal in the input side and the output side. Contact arrangement intervals etc. have also been adjusted so as to be the same at the input side and the output side. With this type of structure, the same current flows in both of the NMOS transistors, and the load is evenly shared between the input side and the output side.

In the second embodiment, in addition to the effects of the first embodiment, the respective pattern layouts of the input side NMOS transistor and the output side NMOS transistor are constructed having the same relationship. In this way, it is possible to improve the resistance to static electricity etc. of the circuit overall.

The ratio of the number of first contacts to the number of second contact in the invention described above is suitably variable according to the desired overall resistance etc., but in order to sufficiently obtain the effects of the present invention, the unit resistance of the first contacts is preferably designed so as to be no more than ten times the unit resistance of the second contacts.

CLAIMS.

Claim 1.

A semiconductor integrated circuit device, comprising:

impurity diffusion regions formed as source and drain on a semiconductor substrate;

a first conductive layer having a first resistivity formed on said impurity diffusion regions;

a first contact hole group connecting said first conductive layer and said impurity diffusion region;

a second conductive layer having a second resistivity formed on said first conductive layer; and

a second contact hole group connecting said first conductive layer and said second conductive layer at an upper part of said impurity diffusion region, wherein

a total number of contact holes is respectively different between said first contact hole group and said second contact hole group.

Claim 2.

The semiconductor integrated circuit device as disclosed in claim 1, wherein said first resistivity is higher than said second resistivity, and a total number of holes in said first contact hole group is more than a total number of holes in said second contact hole group.

Claim 3.

A semiconductor integrated circuit device, comprising:

a source region formed on a semiconductor substrate;

a first conductive layer having a first resistivity formed on said source region;

a first contact hole group connecting said source region and said first conductive layer;

a second conductive layer having a second resistivity formed on said first conductive layer;

a second contact hole group, on an upper part of said source region, connecting said first conductive layer and said second conductive layer;

a drain region formed on a semiconductor substrate;

a third conductive layer having said first resistivity formed on said drain region;

a third contact hole group connecting said drain region and said third conductive layer;

a fourth conductive layer having said second resistivity formed on said third conductive layer;

a fourth contact hole group, on an upper part of said drain region, connecting said third conductive layer and said fourth conductive layer;

wherein

a total number of contact holes is respectively different between said first contact hole group and said third contact hole group, and

a total number of contact holes is respectively different between said second contact hole group and said fourth contact hole group.

Claim 4.

The semiconductor integrated circuit device as disclosed in claim 3, wherein the total number of contact holes in said first contact hole group is the same as the total number of contact holes in said third contact hole group, and the total number of contact holes in said second contact hole group is the same as the total number of contact holes in said fourth contact hole group.

Claim 5.

The semiconductor integrated circuit device as disclosed in claim 4, wherein said first resistivity is higher than said second resistivity, the total number of contact holes for said first contact hole group and said third contact hole group is more than the total number of contact holes for said second contact hole group and said fourth contact hole group.

Claim 6.

A semiconductor integrated circuit device, comprising:

a first impurity diffusion region and a second impurity diffusion region formed on a semiconductor substrate, extending in a first direction and standing

side by side in a second direction;

a first conductive layer having a first resistivity formed on said first impurity diffusion region;

a first contact hole group having a plurality of contact holes arranged side by side in said first direction, for connecting said first impurity diffusion region and said first conductive layer;

a second conductive layer having a second resistivity formed on said first conductive layer;

a second contact hole group, having a plurality of contact holes arranged side by side in said first direction for connecting said first conductive layer and said second conductive layer, at an upper part of said first impurity diffusion region;

a third conductive layer having said first resistivity formed on said second impurity diffusion region;

a third contact hole group having a plurality of contact holes arranged side by side in said first direction, for connecting said second impurity diffusion region and said third conductive layer;

a fourth conductive layer having said second resistivity formed on said third first conductive layer; and

a fourth contact hole group, having a plurality of contact holes arranged side by side in said first direction for connecting said third conductive layer and said fourth conductive layer, at an upper part of said second impurity diffusion region, wherein

said first contact hole group is arranged between neighboring contact holes of said second contact hole group, and

said third contact hole group is arranged between neighboring contact holes of said fourth contact hole group.

Claim 7.

The semiconductor integrated circuit device as disclosed in claim 6, wherein

a distance between a contact hole of said first contact group and a contact hole of said second contact hole group adjacent to the contact hole of said first

contact hole group is a fixed value, and

a distance between a contact hole of said third contact group and a contact hole of said fourth contact hole group adjacent to the contact hole of said third contact hole group is a fixed value.

Claim 8.

The semiconductor integrated circuit device as disclosed in claim 6, wherein

an interval between contact holes of said first contact group situated between neighboring holes of said second contact hole group is a fixed value, and

an interval between contact holes of said third contact group situated between neighboring holes of said fourth contact hole group is a fixed value.

Claim 9.

The semiconductor integrated circuit device as disclosed in claim 6, wherein said first impurity diffusion region has

a first side and a second side running in said second direction,

a third side running in said first direction and opposite to said second impurity diffusion region,

a first distance defined as a distance from said first side to an edge of said first contact hole group extremely close to said first side,

a second distance defined as a distance from said second side to an edge of said first contact hole group extremely close to said second side, and

a third distance defined as a distance from said third side to an edge of said first contact hole group extremely close to said third side

said second impurity diffusion region has

a fourth side and a fifth side running in said second direction,

a sixth side running in said first direction and opposite to said first impurity diffusion region,

a fourth distance defined as a distance from said fourth side to an edge of said third contact hole group extremely close to said fourth side,

a fifth distance defined as a distance from said fifth side to an edge of

said third contact hole group extremely close to said fifth side, and

a sixth distance defined as a distance from said sixth side to an edge of said third contact hole group extremely close to said sixth side, wherein

said first distance and said second distance are both larger than said third distance, and

said fourth distance and said fifth distance are both larger than said sixth distance.

Claim 10.

The semiconductor integrated circuit device as disclosed in claim 6, wherein

said first contact hole group is divided into a plurality of subgroups according to a predetermined fixed number of contact holes, and each subgroup is arranged between adjacent contact holes of said second contact hole group, and

said third contact hole groups are divided into a plurality of subgroups according to a predetermined fixed number of contact holes, and each subgroup is arranged between adjacent contact holes of said fourth contact hole group.

Claim 11.

The semiconductor integrated circuit device as disclosed in claim 10, wherein

a distance from contact holes of said first contact hole group and contact holes of said second contact hole group adjacent to holes of said first contact hole group, has a fixed value and

a distance from contact holes of said third contact hole group and contact holes of said fourth contact hole group adjacent to holes of said third contact hole group, has a fixed value.

Claim 12.

The semiconductor integrated circuit device as disclosed in claim 10, wherein

an interval between contact holes of said first contact hole groups

arranged between adjacent contact holes of said second contact hole group has a fixed value, and

an interval between contact holes of said third contact hole groups arranged between adjacent contact holes of said fourth contact hole group has a fixed value.

Claim 13.

The semiconductor integrated circuit device as disclosed in claim 10, wherein

said first impurity diffusion region has

a first side and a second side running in said second direction,

a third side running in said first direction and opposite to said second impurity diffusion region,

a first distance defined as a distance from said first side to an edge of said first contact hole group extremely close to said first side,

a second distance defined as a distance from said second side to an edge of said first contact hole group extremely close to said second side, and

a third distance defined as a distance from said third side to an edge of said first contact hole group extremely close to said third side

said second impurity diffusion region has

a fourth side and a fifth side running in said second direction,

a sixth side running in said first direction and opposite to said first impurity diffusion region,

a fourth distance defined as a distance from said fourth side to an edge of said third contact hole group extremely close to said fourth side,

a fifth distance defined as a distance from said fifth side to an edge of said third contact hole group extremely close to said fifth side, and

a sixth distance defined as a distance from said sixth side to an edge of said third contact hole group extremely close to said sixth side, wherein

said first distance and said second distance are both larger than said third distance, and

said fourth distance and said fifth distance are both larger than said sixth

distance.

Claim 14.

A semiconductor integrated circuit, comprising a first transistor for input and a second transistor for output, said first transistor and said second transistor being connected to an input/output terminal, said first transistor comprising:

a first impurity diffusion region and a second impurity diffusion region formed on a semiconductor substrate, extending in a first direction and standing side by side in a second direction;

a first conductive layer having a first resistivity formed on said first impurity diffusion region;

a first contact hole group having a plurality of contact holes arranged side by side in said first direction, for connecting said first impurity diffusion region and said first conductive layer;

a second conductive layer having a second resistivity formed on said first conductive layer;

a second contact hole group, having a plurality of contact holes arranged side by side in said first direction for connecting said first conductive layer and said second conductive layer, at an upper part of said first impurity diffusion region;

a third conductive layer having said first resistivity formed on said second impurity diffusion region;

a third contact hole group having a plurality of contact holes arranged side by side in said first direction, for connecting said second impurity diffusion region and said third conductive layer;

a fourth conductive layer having said second resistivity formed on said third first conductive layer; and

a fourth contact hole group, having a plurality of contact holes arranged side by side in said first direction for connecting said third conductive layer and said fourth conductive layer, at an upper part of said second impurity diffusion region, wherein

said first contact hole group has a predetermined fixed number of contact

holes arranged between each neighboring contact hole of said second contact hole group, and has a first fixed interval between said predetermined number of arranged contact holes and adjacent contact holes, and

said third contact hole group has a predetermined fixed number of contact holes arranged between each neighboring contact hole of said fourth contact hole group, and has said first fixed interval between said predetermined number of arranged contact holes and adjacent contact holes, and said second transistor comprising:

a third impurity diffusion region and a fourth impurity diffusion region formed on a semiconductor substrate, extending in a third direction and standing side by side in a fourth direction;

a fifth conductive layer having a first resistivity formed on said third impurity diffusion region;

a fifth contact hole group having a plurality of contact holes arranged side by side in said third direction, for connecting said third impurity diffusion region and said fifth conductive layer;

a sixth conductive layer having a second resistivity formed on said fifth conductive layer;

a sixth contact hole group, having a plurality of contact holes arranged side by side in said third direction for connecting said fifth conductive layer and said sixth conductive layer, at an upper part of said third impurity diffusion region;

a seventh conductive layer having said first resistivity formed on said fourth impurity diffusion region;

a seventh contact hole group having a plurality of contact holes arranged side by side in said third direction, for connecting said fourth impurity diffusion region and said seventh conductive layer;

an eighth conductive layer having said second resistivity formed on said seventh first conductive layer; and

an eighth contact hole group, having a plurality of contact holes arranged side by side in said third direction for connecting said seventh conductive layer and said eighth conductive layer, at an upper part of said fourth impurity diffusion region, wherein

said fifth contact hole group has a predetermined fixed number of contact holes arranged between each neighboring contact hole of said sixth contact hole group, and has said first fixed interval between said predetermined number of arranged contact holes and adjacent contact holes, and

said seventh contact hole group has a predetermined fixed number of contact holes arranged between each neighboring contact hole of said eighth contact hole group, and has said first fixed interval between said predetermined number of arranged contact holes and adjacent contact holes.

Claim 15.

The semiconductor integrated circuit as disclosed in claim 14, having

a first side, for said first impurity diffusion region, running in said first direction and opposite to said second impurity diffusion region;

a second side, for said second impurity diffusion region, running in said first direction and opposite to said first impurity diffusion region;

a third side, for said third impurity diffusion region, running in said third direction and opposite to said fourth impurity diffusion region;

a fourth side, for said fourth impurity diffusion region, running in said third direction and opposite to said third impurity diffusion region;

a first distance defined as a distance between said first side and said second side; and

a second distance defined as a distance between said third side and said fourth side, wherein

said first distance and said second distance are equal.

ABSTRACT

An increase in overall resistance value is prevented by having different contact resistance connecting between different wiring layers. A transistor has a first conductive layer having a first resistivity formed on an impurity diffusion regions, a first contact hole group connecting the first conductive layer and the impurity diffusion region, a second conductive layer having a second resistivity formed on the first conductive layer, and a second contact hole group connecting the first conductive layer and the second conductive layer at an upper part of the impurity diffusion region. The first contact hole group and the second contact hole group have a different total number of contact holes.

Fig.1

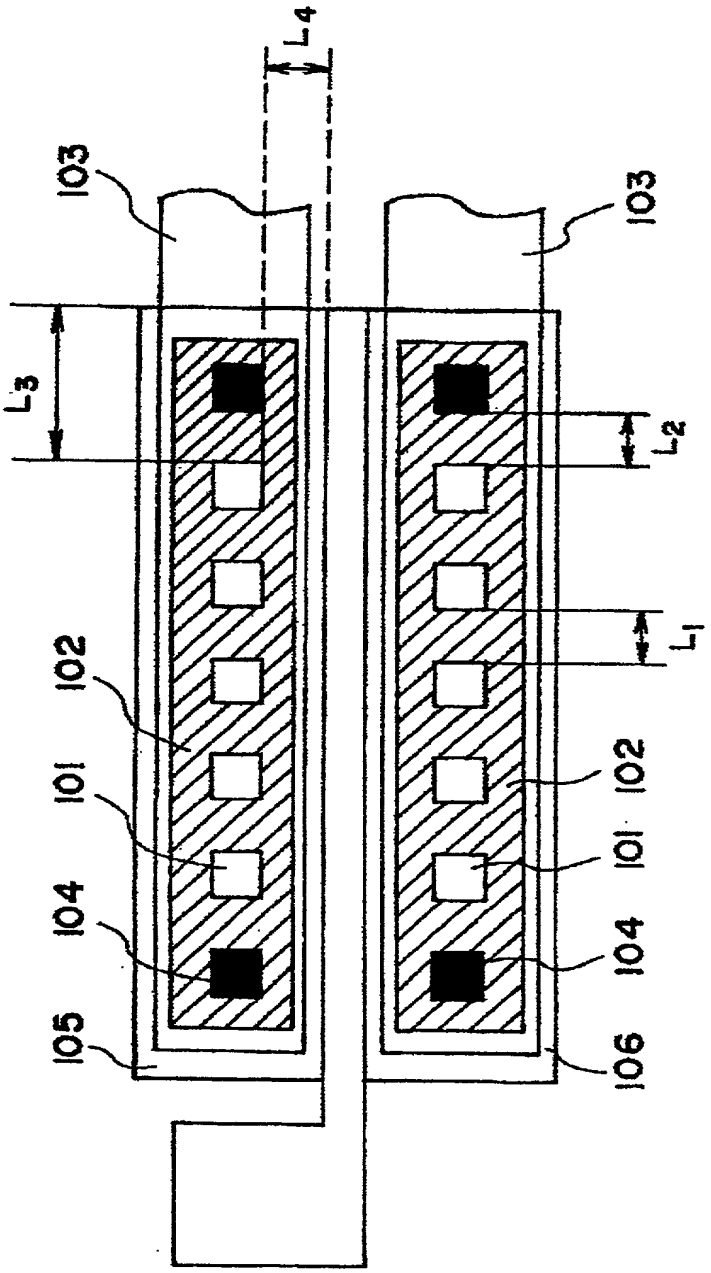


Fig.2

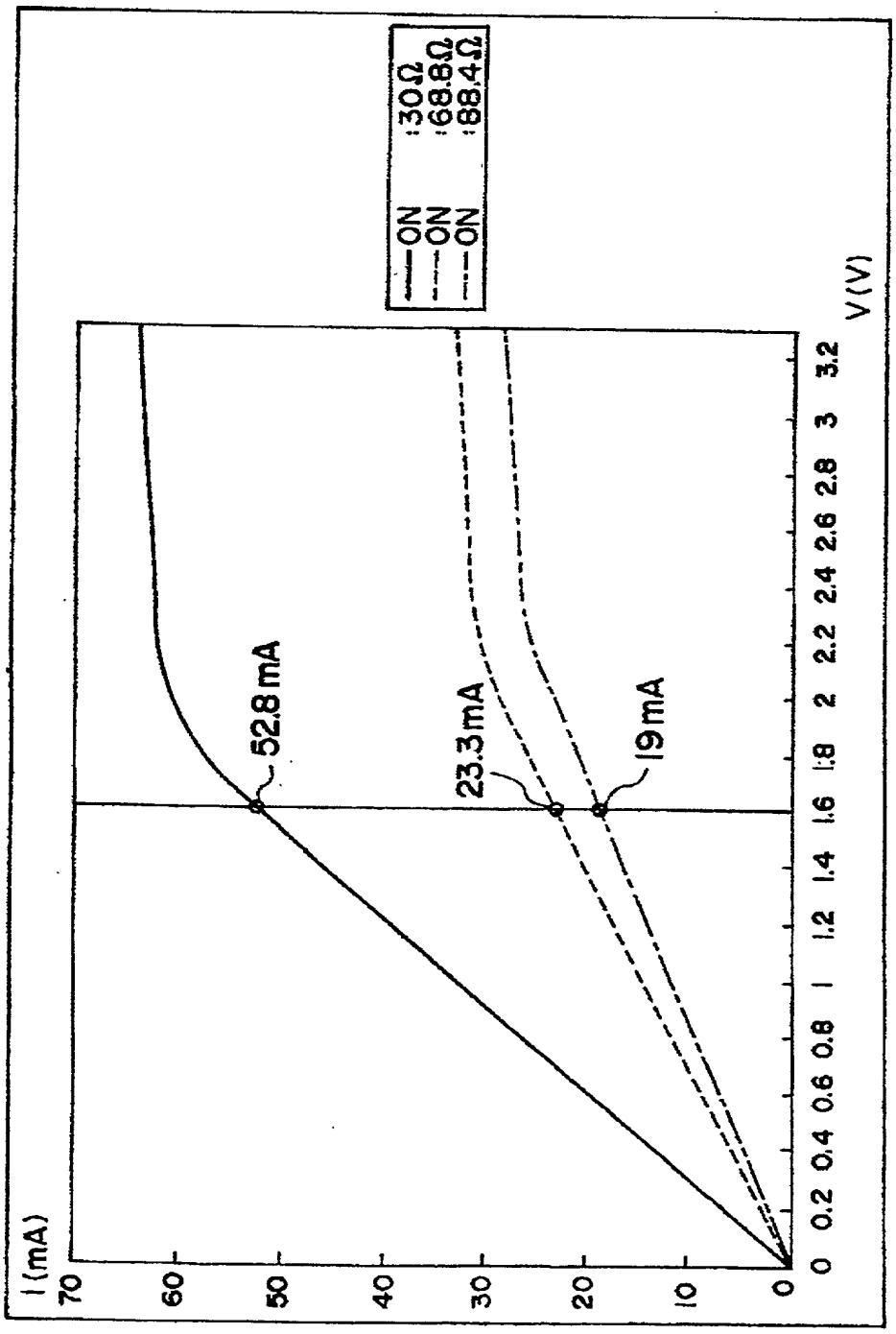

I(mA)
70
60
50
40
30
20
10
0
0 0.2 0.4 0.6 0.8 1 1.2 1.4 1.6 1.8 2 2.2 2.4 2.6 2.8 3 3.2
V(V)
52.8mA
23.3mA
19mA
ON 30Ω
ON 68.8Ω
ON 88.4Ω

Fig.3

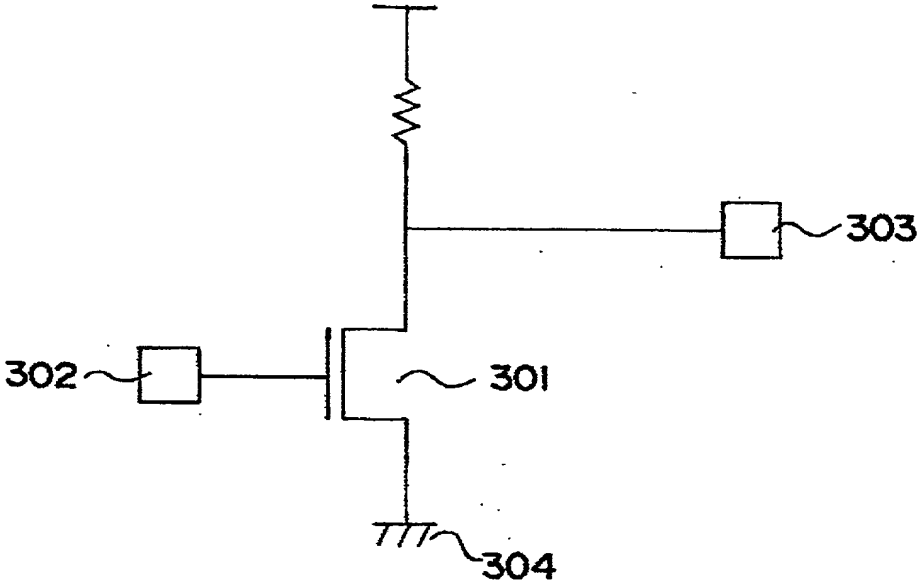
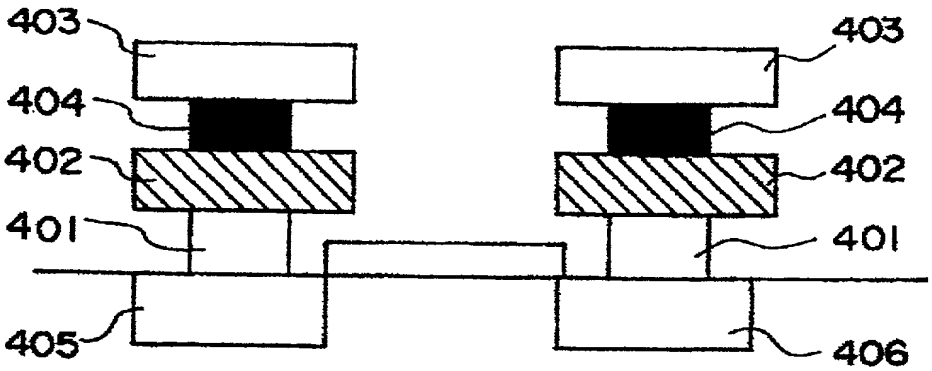
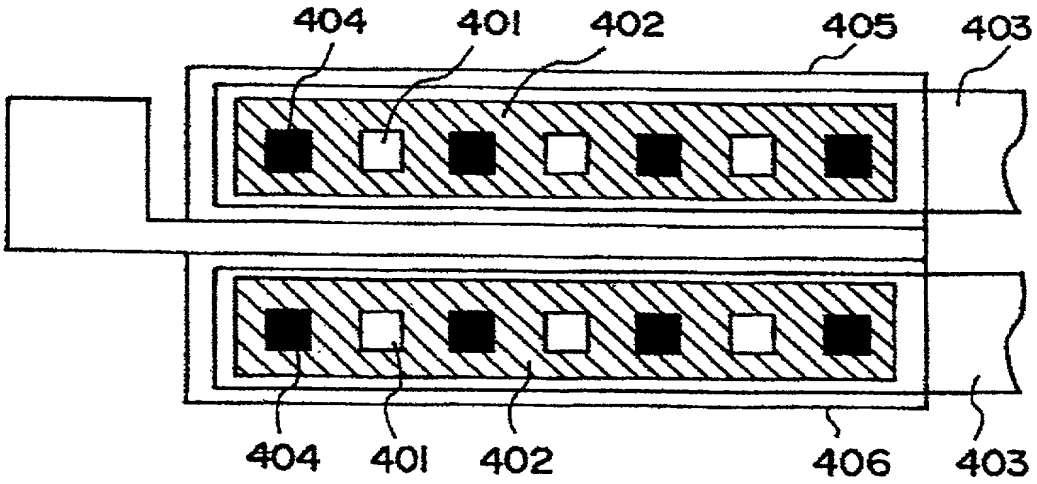


Fig.4

(A)

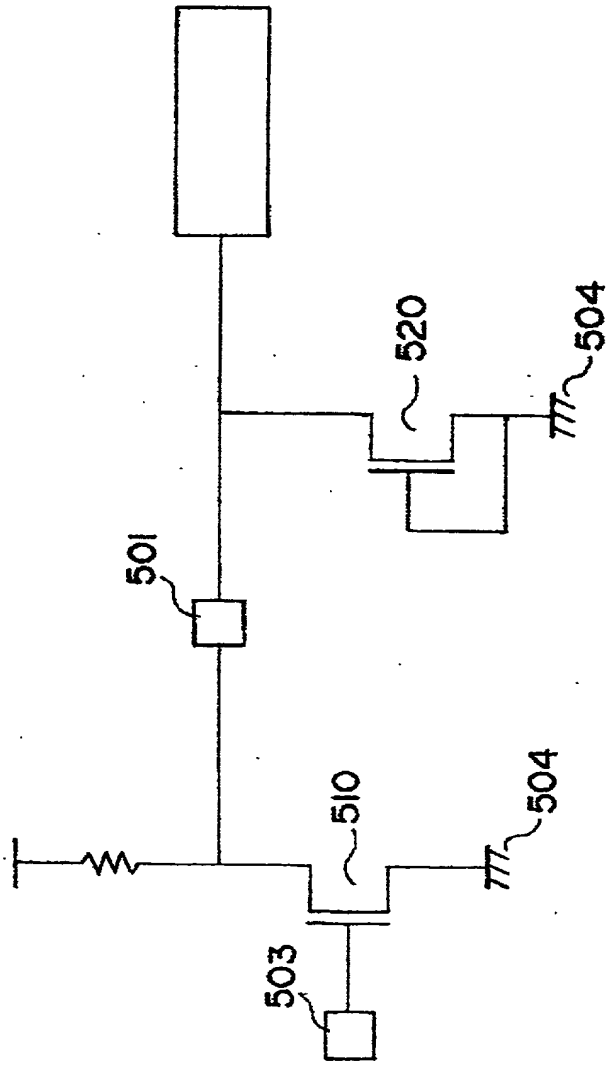


(B)



0922606.041396

Fig.5



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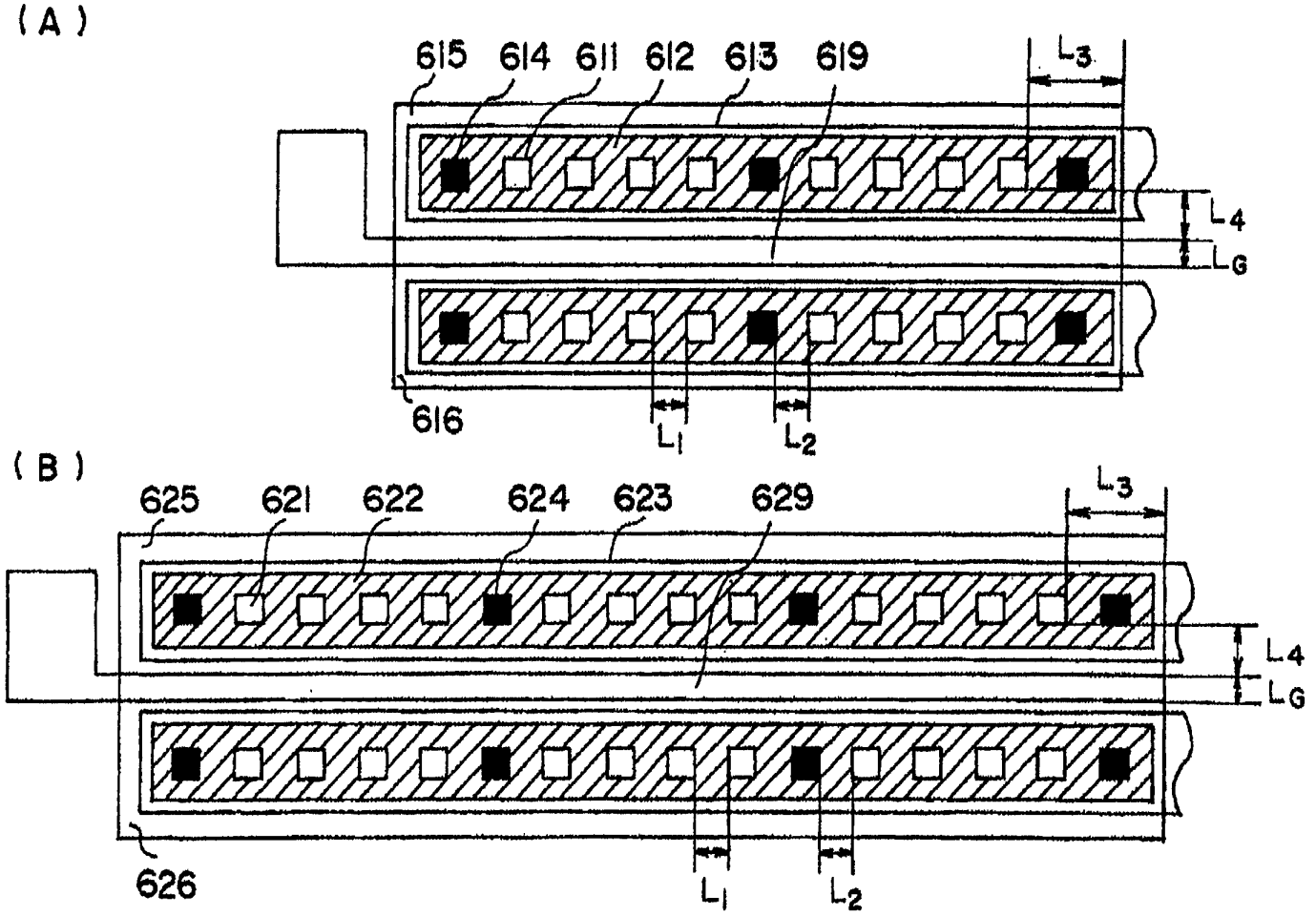

Fig.6

2/95b DECLARATION FOR UNITED STATES PATENT APPLICATION, POWER OF ATTORNEY, DESIGNATION OF CORRESPONDENCE ADDRESS

Attorney Docket OKI 4646.01

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and that I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SEMICONDUCTOR INTEGRATED CIRCUIT

the specification of which

[X] is attached hereto.

[ ] was filed on _____ as Application No. _____ and was amended on _____ [if applicable].

[ ] was filed under the Patent Cooperation Treaty on _____, Serial No. _____, the United States of America being designated.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent, utility model, design or inventor's certificate listed below and have also identified below any foreign application(s) for patent, utility model, design or inventor's certificate having a filing date before that of the application(s) on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Date Filed	Yes	No
21021/98	JAPAN	January 23, 1998	X	

I hereby appoint the following attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: George H. Spencer (Reg. No. 18,038), Norman N. Kunitz (Reg.No. 20,586), Robert J. Frank (Reg. No. 19,112), Gabor J. Kelemen (Reg. No. 21,016), Robert Kinberg (Reg. No. 26,924), John W. Schneller (Reg. No. 26,031), Ashley J. Wells (Reg. No. 29,847), Christopher H. Lynt (Reg. No. 33,619) 1100 New York Avenue, N.W., Suite 300 East, Washington, D.C. 20005-3955, Telephone: (202) 414-4000, Telefax: (202) 414-4040. Address all correspondence to SPENCER & FRANK 1100 New York Ave., N.W., Suite 300 East, Washington, D.C. 20005-3955.

The undersigned hereby authorizes the U.S. attorneys named herein to accept and follow instructions from the undersigned's assignee, if any, and/or, if the undersigned is not a resident of the United States, the undersigned's domestic attorney, patent attorney or patent agent, as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U.S. attorneys and the undersigned. In the event of a change in the person(s) from whom instructions may be taken, the U.S. attorneys named herein will be so notified by the undersigned.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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